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TITLE: Method for manufacturing semiconductor device

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PATENT-FAMILY:

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| KR 403992 B | November 3, 2003 | N/A | 000 | H01L 029/78 |
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INT-CL (IPC): H01L029/78

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BASIC-ABSTRACT:

NOVELTY - A fabrication method of a semiconductor device is provided to restrain a formation of pores by using an RF(Radio Frequency) plasma cleaning when fabricating an FET(Field Effect Transistor) having an ESD(Elevated Source and Drain) structure.

DETAILED DESCRIPTION - A gate insulating layer(106) is formed at an active region(102) of a silicon substrate(101). A gate electrode(108) is formed on the gate insulating layer(106). A gate oxide(110) is formed at both sidewalls of the gate electrode(108) by oxidation of the gate electrode. An LDD(Lightly Doped Drain) region(112) is formed in the silicon substrate(101) by implanting lightly doped dopants. A nitride gate spacer(114) is formed at both sidewalls of the gate oxide(110). Then, the resultant structure is cleaned by an RF(Radio Frequency) plasma using SF₆ gas. A silicon epitaxial layer grows on the entire surface of the resultant structure.

SF₆ 플라즈마 세정

